REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Official Action dated May 3, 2004, the Examiner rejected Claims 1-9 under 35 U.S.C. §112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Particularly, in Claims 1 and 9, the Examiner alleges the "pipeline" lacks antecedent basis. In response, applicants amend their respective preambles to set forth a pipeline providing the antecedent basis for the later recitation of "the pipeline". Particularly, in the invention, a multistage pipeline for the rename process controlling the out-of-order issue of instructions is provided. For example, in Figure 5, a multi stage pipeline is show in which the rename process controlling the out-of-order issue of instruction consists of the stages "ren", "read ROB", "write RS" followed by "select" and "issue".

Further, in Claim 1, the Examiner alleges that it is not clear what is dependent on what for the recited "dependency conflict". In response, applicants amend the element of Claim 1 to recite that the "dependency conflict" refers to those conflicts that may arise between instructions processed in program order in said pipeline. That is, in the context of the present invention, the term dependency refers to a relationship between a first and a subsequent instruction in program order which requires the execution of the first instruction prior to the execution of the sebsequent instruction. In the invention, one type of a conflict refers to operand dependencies. An operand dependency occurs if a source

operand of the second instruction is the result of the first instruction. A so called read-after-write conflict occurs when a second instruction (which needs to read the operand data of previous instructions) is issued before the result of the first instruction is available (or has written its results). In other words, in the Read-after-Write conflict case the second instruction is issued for execution without all operand data being available, hence the execution result will not be valid.

Further, in Claim 1, the Examiner alleges that it is not clear what stages are in the pipeline, and what it means to "process the pipeline in a compressed way" and further, that it is unclear how dependency conflict is risked. Applicants respond as follows: In the present invention, as set forth in Claim 1, the recitation "process the pipeline in a compressed way risking dependency conflicts" means the use of a shorter pipeline in which no longer all Read-after-Write operand dependency conflicts are resolved. Hence, instructions with read-after-write conflicts may be issued (the "risk"). This occurs in the present invention for cases that are rather seldom to occur. Therefore, having the shorter pipeline together with having additional logic detecting/resolving the operand dependency Read-after-Write conflict (followed by, for example, the re-issue of the instruction result in a better performance as using a longer pipeline that never issues an instruction with a read-after-write conflict).

In the Office Action, the Examiner alleges that Claims 7 and 9 have similar problems as in Claim 1. Applicants hereby amend Claim 7 and 9 accordingly to correct the informalities indicated by the Examiner in these claims.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw rejection of independent Claims 1, 7 and 9, and their respective dependent claims under 35 USC §112, second paragraph.

With respect to the prior art made of record by the Examiner and not relied upon, applicants submit that the patents Hesson et al (US 5,625,789), Martell et al (US 5,546,597), and Witt et al (US 6,122,727), each teach prior art techniques, including the operand dependency analysis (i.e. detecting Read-after-Write conflicts for the operand dependencies) whereby the conflict dependency analysis is always "complete" such that an instruction with a Read-after-Write conflict is never issued. For high frequency processor such a complete resolving operand dependency analysis leads to a very long pipeline (like for example the prior art pipeline in Fig 3.). In the present invention, the claimed "process the pipeline in a compressed way risking dependency conflicts" means the use of a shorter pipeline in which no longer all Read-after-Write operand dependency conflicts are resolved as explained hereinabove. It should be noted that the operand read-after-write conflict is different from the rapid pipeline recovery as for example presented by Witt for branch mis-predicts and well as load/store conflicts. None of the prior art references allow instructions with operand dependency conflicts be issued.

In summary, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with

the Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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